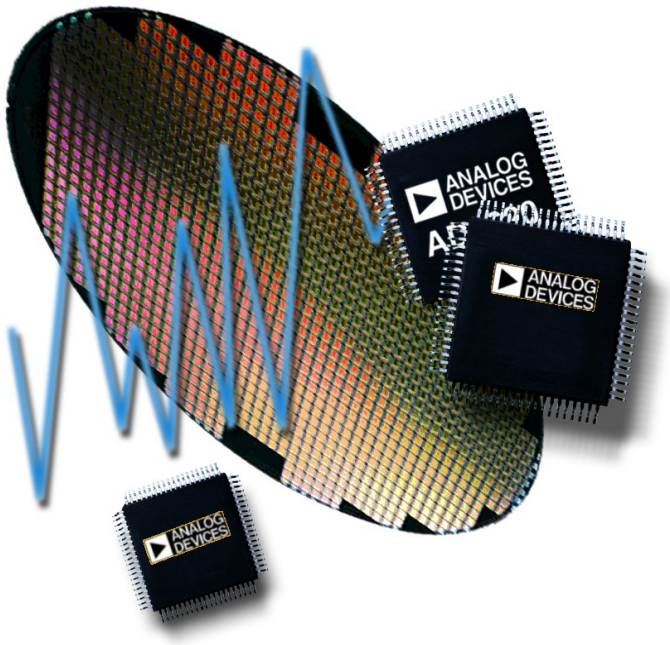

Reliability Report

Report Title: ADRF5020/21/26/27 Laminate Vendor Change Qualification

Report Number: 19328

Revision: A

Date: 19 December 2024

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADRF5020, ADRF5021, ADRF5026, and ADRF5027 products – each packaged individually in a 20-LGA package with the new Daeduck laminate.

Die/Fab Product Characteristics

Table 1: Die/Fab Product Characteristics- 0.18um CMOS

Product Characteristics	Products to be qualified			
Generic/Root Part #	ADRF5021	ADRF5020	ADRF5027	ADRF5026
Die Id	01CK521 / 01CK549	01CK521 A	01LN595 01LN707	01LN595 A
Die Size (mm)	1.40 x 2.15	1.40 x 2.15	1.40 x 2.15	1.40 x 2.15
Wafer Fabrication Site	E_GLBX0908	E_GLBX0908	E_GLBX0908	E_GLBX0908
Wafer Fabrication Process	0.18um CMOS	0.18um CMOS	0.18um CMOS	0.18um CMOS
Die Substrate	Si	Si	Si	Si
Polyimide	No	No	No	No
Passivation	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN	undoped-oxide/SiN

Package/Assembly Product Characteristics

Table 2: Package/Assembly Product Characteristics - 20-LGA at ASE (AEK)

Product Characteristics	Products to be qualified			
Generic/Root Part #	ADRF5020	ADRF5021	ADRF5026	ADRF5027
Package	20-LGA	20-LGA	20-LGA	20-LGA
Body Size (mm)	3.00 x 3.00 x 0.73	3.00 x 3.00 x 0.73	3.00 x 3.00 x 0.73	3.00 x 3.00 x 0.73
Assembly Location	ASE (AEK)	ASE (AEK)	ASE (AEK)	ASE (AEK)
MSL/Peak Reflow Temperature(°C)	3 / 260°C	3 / 260°C	3 / 260°C	3 / 260°C
Mold Compound	Hitachi CEL9700ZHF10-UG2	Hitachi CEL9700ZHF10-UG2	Hitachi CEL9700ZHF10-UG2	Hitachi CEL9700ZHF10-UG2
Laminate Stack	2-Layer Laminate	2-Layer Laminate	2-Layer Laminate	2-Layer Laminate

Package/Assembly Test Results

Table 3: Package/Assembly Test Results - LGA at ASE (AEK)

Test Name	Spec	Conditions	Generic/Root Part #	Lot #	Fail/SS
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADRF5020	Q19328.1.HS1	0/77
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 96 Hours	ADRF5020	Q19328.1.HA1	0/77
			ADRF5021	Q19328.1.HA2	0/77
			ADRF5027	Q19328.1.HA3	0/77
Low Temperature Storage (LTS)	JESD22-A119	-55°C, 1,000 Hours	ADRF5026	Q19328.1.LS1	0/77
				Q19328.2.LS2	0/77
			ADRF5027	Q19328.2.LS3	0/77
Solder Heat Resistance (SHR)	J-STD-020	MSL-3	ADRF5020	Q19328.1.SH1	0/11
			ADRF5021	Q19328.1.SH2	0/11
			ADRF5027	Q19328.1.SH3	0/11
Temperature Cycling (TC)[1]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	ADRF5020	Q19328.1.TC1	0/77
			ADRF5021	Q19328.1.TC2	0/77
			ADRF5027	Q19328.1.TC3	0/77
		-65°C/+150°C, 1,000 Cycles	ADRF5026	Q19328.1.TC4	0/77
				Q19328.2.TC5	0/77
			ADRF5027	Q19328.1.TC6	0/77
Unbiased HAST (UHST)[1]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADRF5026	Q19328.1.UH1	0/77
				Q19328.2.UH2	0/77
			ADRF5027	Q19328.1.UH3	0/77

[1] These samples were subjected to preconditioning at MSL 3 with 3x reflow peak temp of 260°C prior to the start of the stress test.

ESD and Latch-Up Test Results

Table 4: ESD Test Result

ESD Model	Generic/Root Part #	Package	ESD Test Spec	RC Network	Highest Pass Level	Class
FICDM	ADRF5020	20-LGA	JS-002	1Ω, Cpkg	±1250V	C3
	ADRF5021					
	ADRF5026					
	ADRF5027					

Latch-Up testing was not performed. The ADRF5020/21/26/27 are built on a dielectrically isolated wafer fabrication process that is not susceptible to the latch-up phenomenon.

Approvals

Reliability Engineer: Robert Parker-Mason